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Claims

[c1] 1. A layout method for supporting a plurality of CPUs of different package techniques, comprising:
providing a plurality of printed circuit boards;
placing on said printed circuit board that is used to constitute a top signal layer and a bottom signal layer, wherein said placement can be processed on said top signal layer and said bottom signal layer in said area where said control chip is coupled to the CPU;
cutting said printed circuit board that is used to constitute a power layer to cut off an area that is coupled to a reference potential on said power layer in said area where said control chip is coupled to the CPU; and
combining said printed circuit board to form a stack structure.

[c2] 2. The layout method of claim 1, wherein said stack structure comprises:
said top signal layer, used to place a first signal line in said area where said CPU is coupled to the control chip;
a reference potential providing layer, located below said top signal layer, coupled to the reference potential;
a power layer, located below said reference potential

providing layer, comprising:
a voltage providing area for providing an operating voltage to the CPU and said control chip; and
a reference potential providing area, coupled to the reference potential; and
said bottom signal layer, located below said power layer, used to place a second signal line in said area where said CPU is coupled to the control chip.

[c3] 3. The layout method of claim 1, wherein said first signal line refers to the reference potential providing layer.

[c4] 4. The layout method of claim 1, wherein said second signal line refers to the reference potential providing area of said power layer.

[c5] 5. The layout method of claim 1, wherein said stack structure is located in said area where said plurality of signals of said CPU is coupled to the plurality of signals of said control chip.

[c6] 6. The layout method of claim 5, wherein said layout structure is placed on said motherboard.

[c7] 7. The layout method of claim 1, wherein said reference potential is a grounded potential.

[c8] 8. The layout method of claim 1, wherein said reference

potential providing area is located in a first side of said control chip, and said CPU operating voltage providing area cuts into a second side of said control chip.

[c9] 9. The layout method of claim 8, wherein said first side is said side nearest to the CPU, and said second side is a contiguous side of said first side.

[c10] 10. The layout method of claim 1, wherein said CPU is either a CPU that has 423 pins and uses said pin grid array (PGA) package, or a CPU that has 478 pins and uses said ball grid array (BGA) package.

[c11] 11. The layout method of claim 10, wherein said CPU having 423 pins and said CPU having 478 pins use a single control chip to support said CPU operation.